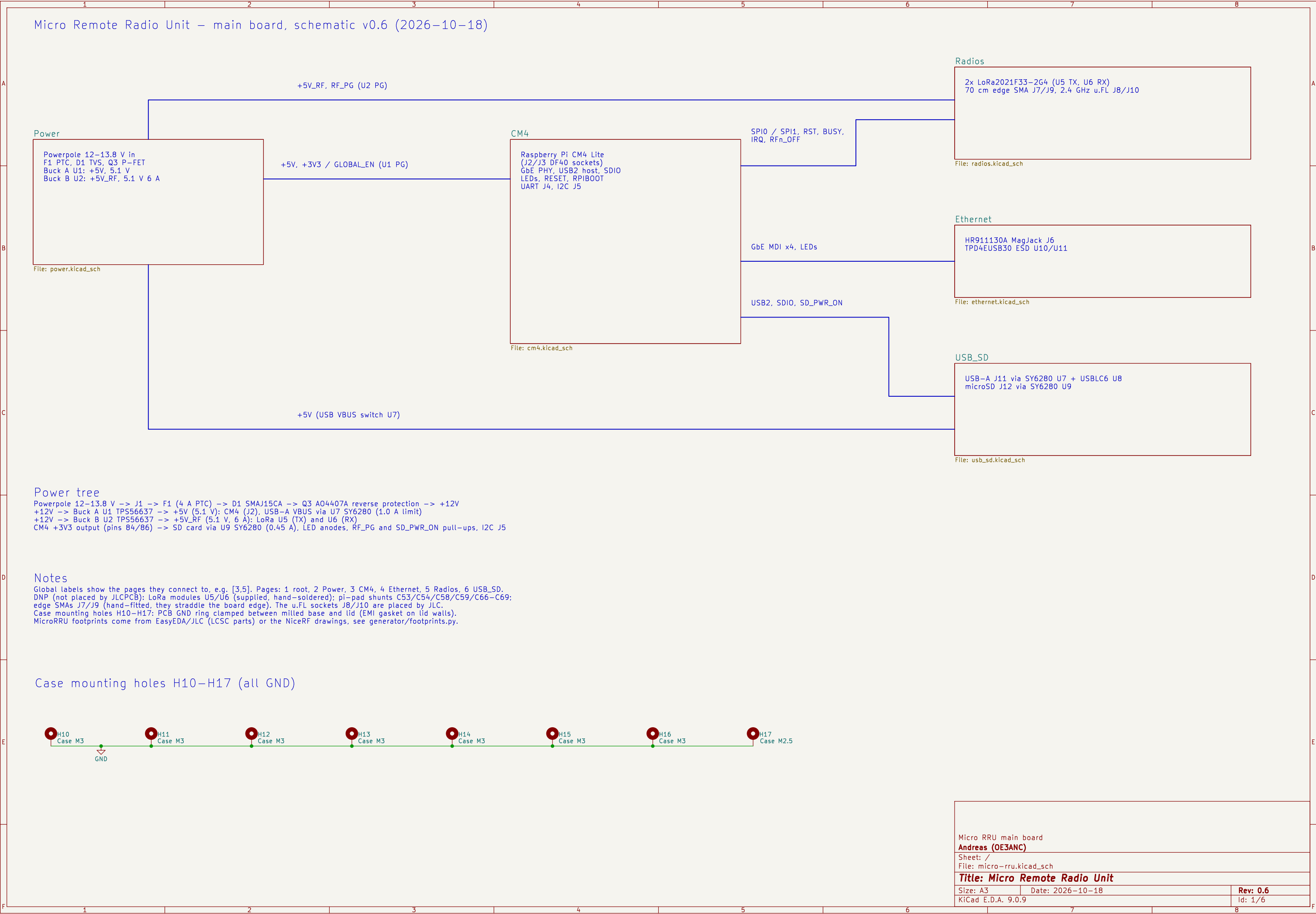
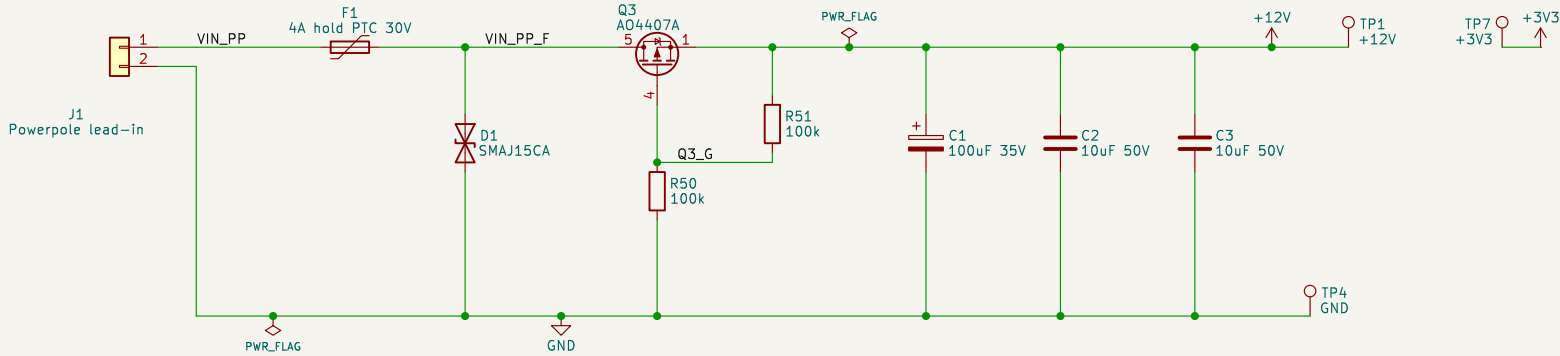




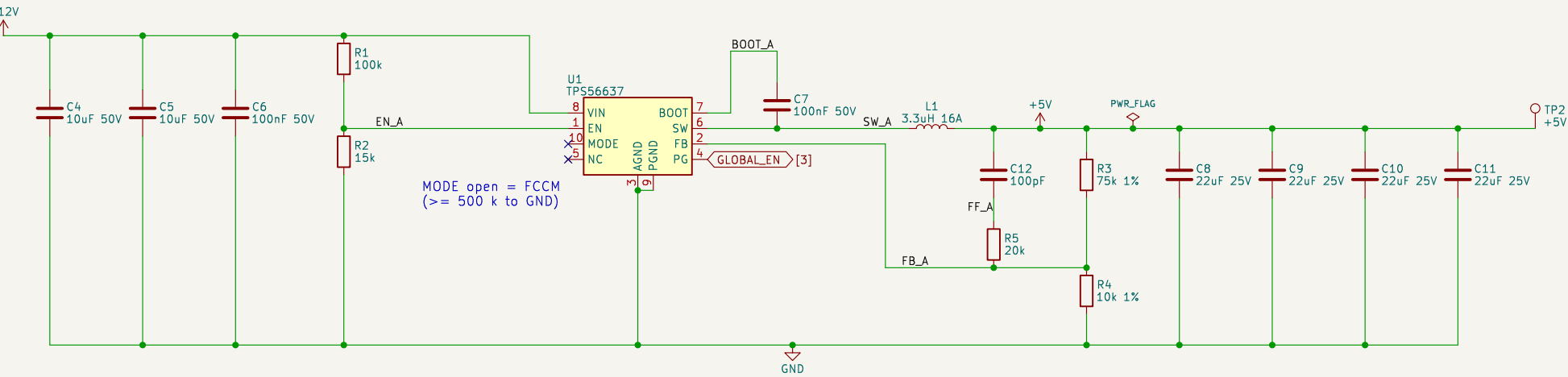
Power input: Powerpole lead-in, fuse, TVS, reverse-polarity P-FET



Powerpole 12–13.8 V only. Reverse polarity: P-FET Q3 in the + lead (body diode forward, then enhanced). Gate divider R50/R51 sets $V_{gs} = -V_{in}/2$: -6 V at 12 V, -12 V at the 24 V TVS clamp (AO4407A V_{gs} max 20–25 V). TP7 (+3V3) is the CM4 3.3 V output, for measurement only.

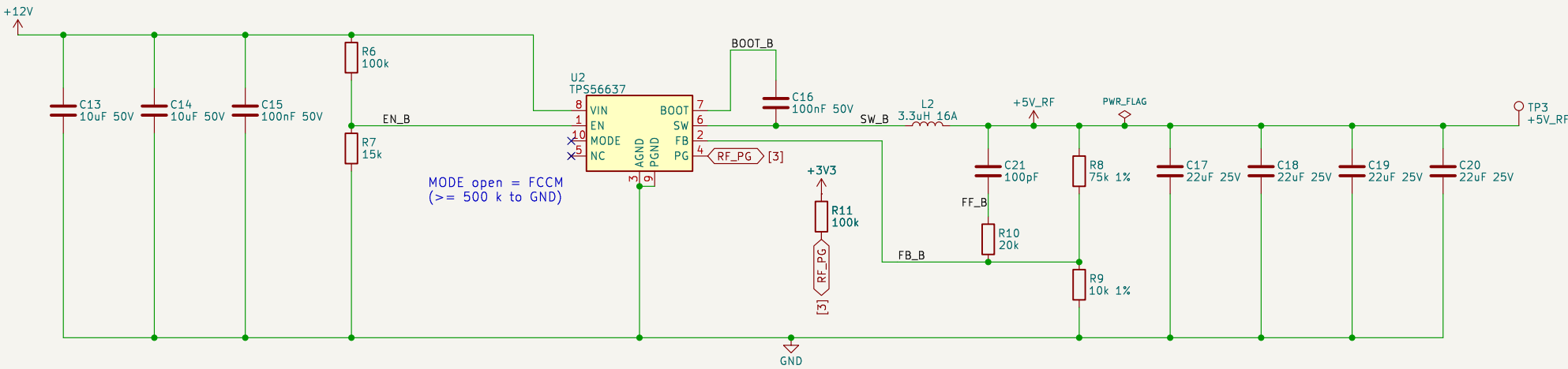
Buck A: +5V (5.1 V) for the CM4 and USB

U1 PG drives CM4 GLOBAL_EN (the CM4 has an internal 100k pull-up to +5V).



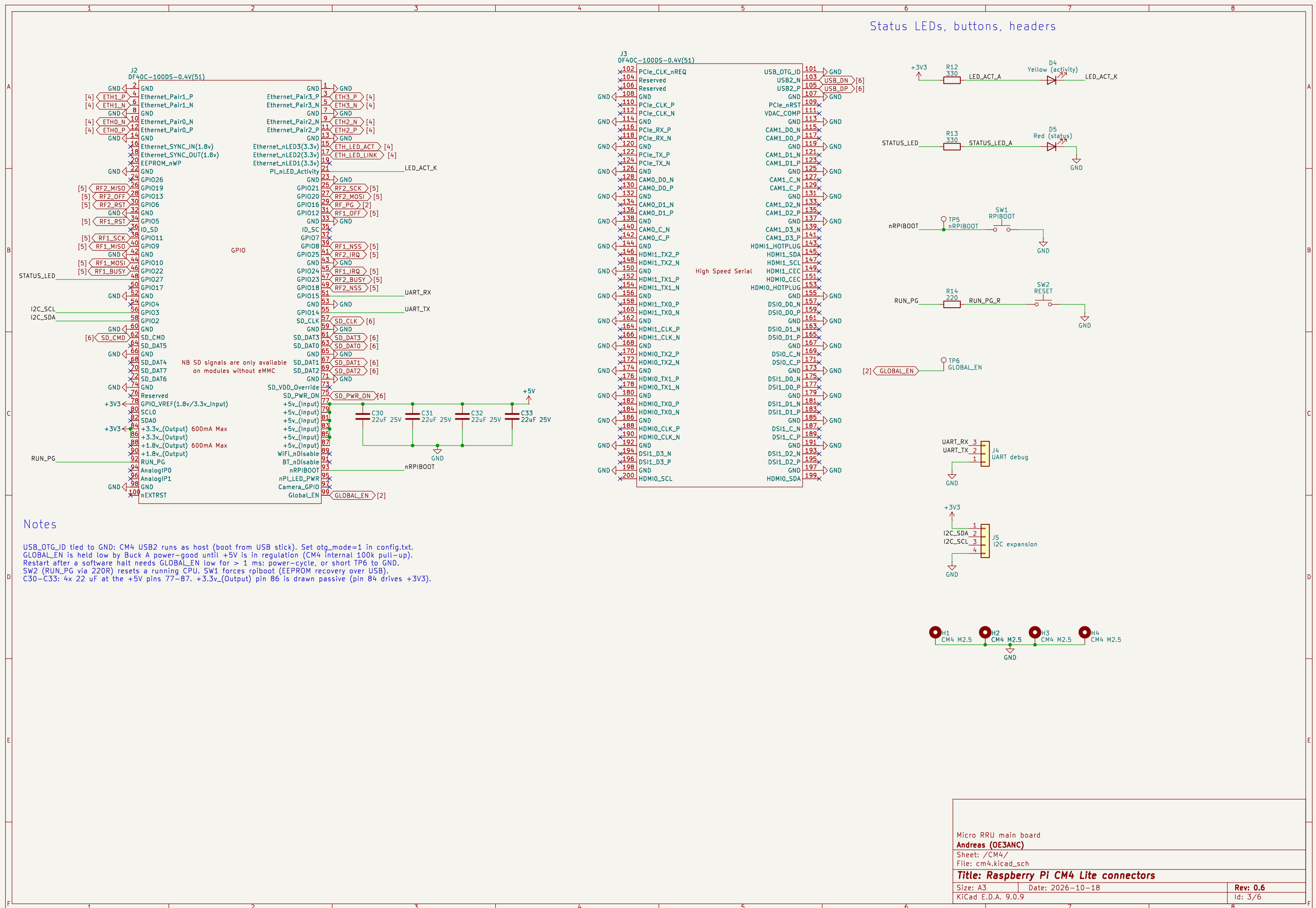
Buck B: +5V_RF (5.1 V, 6 A) for the LoRa PAs

Separate rail keeps PA current steps off the CM4 supply (module VCC 3.0–5.5 V). RF_PG to CM4 GPIO16, R11 pull-up to +3V3.



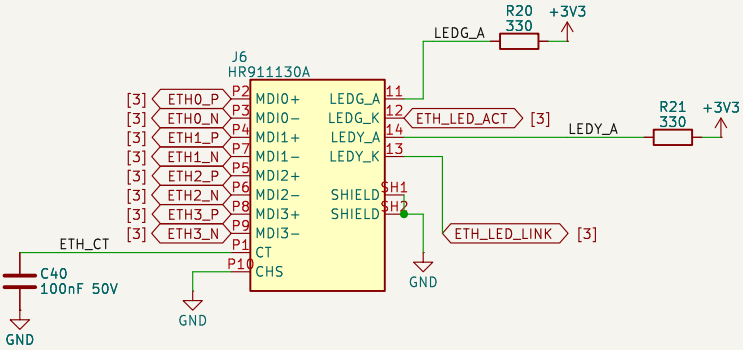
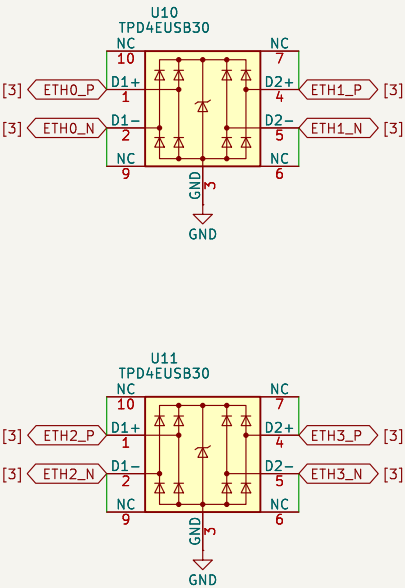
Notes

EN divider 100k/15k (TI SLVSEG1A: VEN rising 1.18 V, I_p 1 uA): starts at -9.0 V typical, 9.6 V max; stops at -8.1 V. EN = 3.7 V at 28 V in (abs max 6 V). MODE open (≥ 500 k) selects FCCM: fixed switching frequency, lower RF noise. Pin 5 is NC (keep floating). Feedback: $V_{out} = 0.6 \text{ V} \times (1 + R_{top} / 10k)$; 75k $\rightarrow$ 5.1 V on both rails (TI table 4). Feed-forward 100 pF + 20k per TI fig. 17. C12/C21 (feed-forward) are 100 pF COG 50 V. L1/L2: 3.3 uH, $I_{sat} \geq 8$ A, DCR < 15 mOhm.



ESD arrays on the PHY side

MagJack, centre tap and LEDs



Notes

U10/U11 (TPD4EUSB30) are flow-through: each pair runs straight across a pad pair (1-10, 2-9, 4-7, 5-6). The pins named NC therefore carry the pair on purpose (wired to their partner pins). Place them behind the jack. Chip-side centre taps (P1) to GND via 100 nF, as on the CM4IO board (C1 on its MagJack). Bob Smith termination (4x 75R + 1 nF 2 kV) is inside the HR911130A; P10 is its chassis end, tied to GND. LEDs: anodes via 330R to +3V3, cathodes to the CM4 nLED outputs (active low), as on CM4IO.

Micro RRU main board

Andreas (OE3ANC)

Sheet: /Ethernet/

File: ethernet.kicad_sch

Title: Gigabit Ethernet MagJack (no PoE)

Size: A4

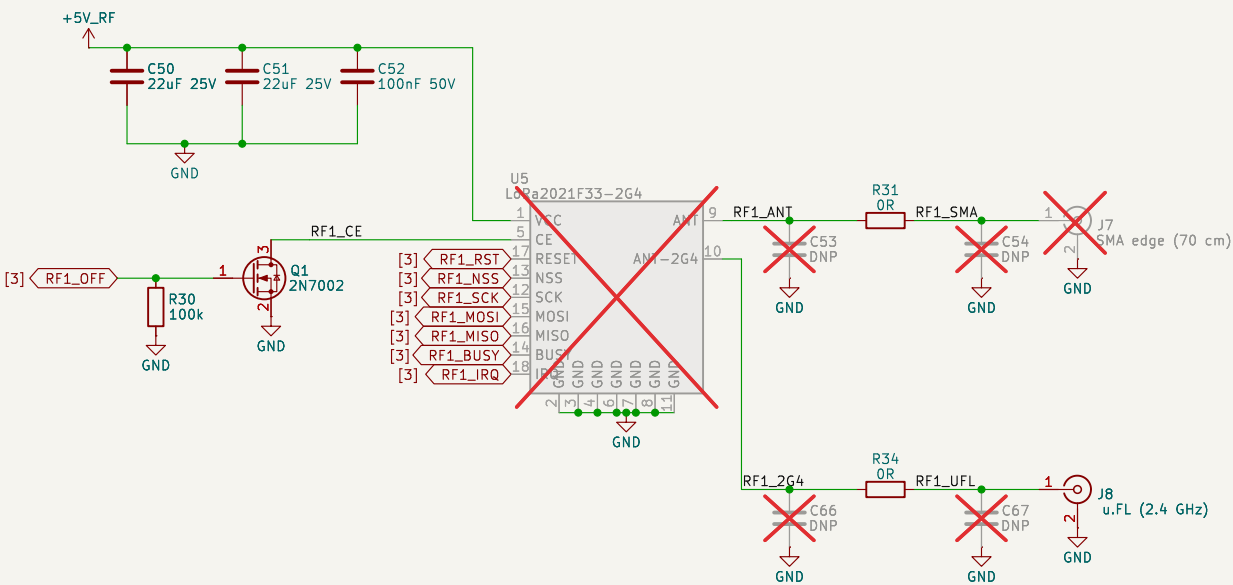
Date: 2026-10-18

Rev: 0.6

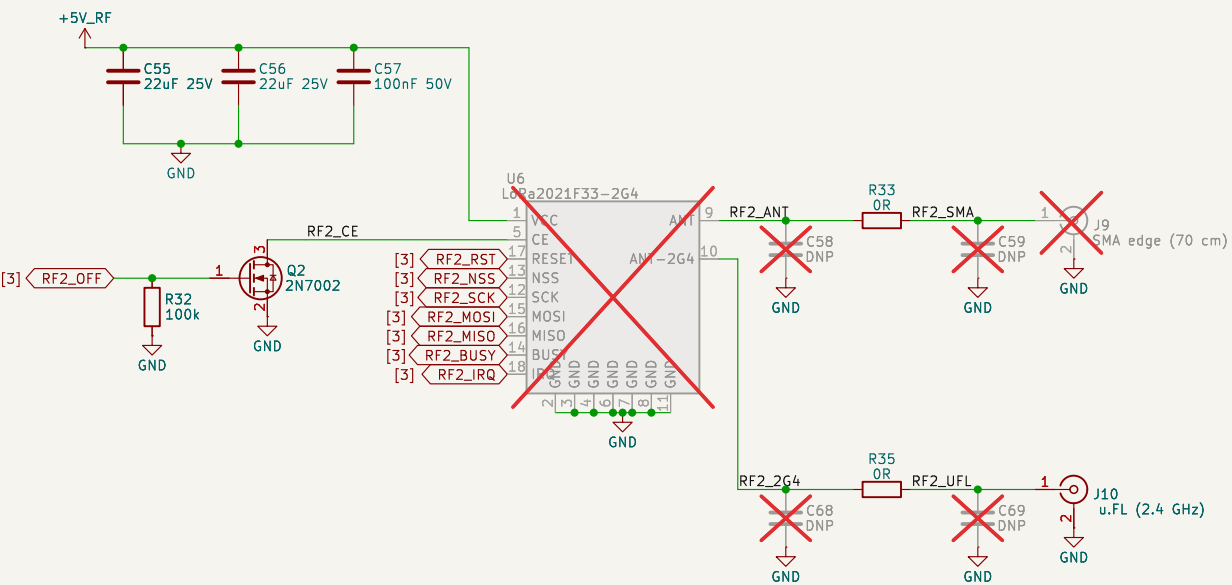
KiCad E.D.A. 9.0.9

Id: 4/6

LoRa module 1: TX (70 cm, to duplexer TX port)



LoRa module 2: RX (70 cm, from duplexer RX port)

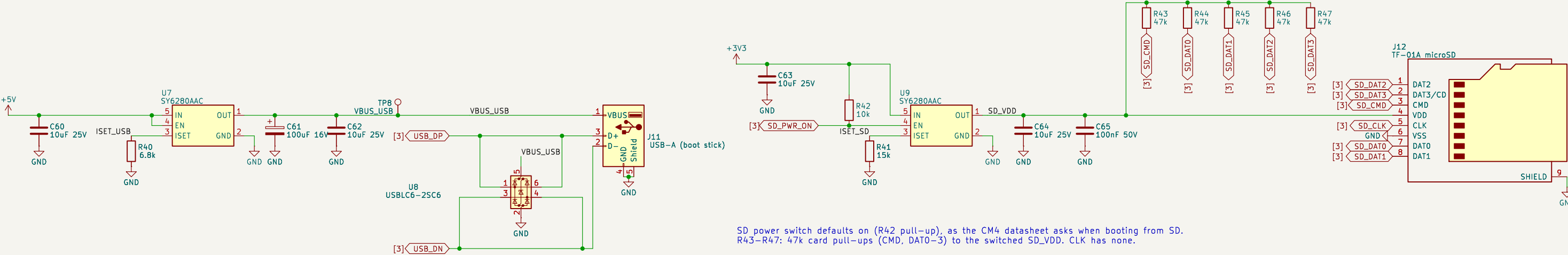


Notes

RFn_OFF high -> CE low -> module LDO off (CE has an internal pull-up; module on by default).
Keep NSS/RESET low while a module is off (datasheet; avoids leakage).
Pi pads: series 0R fitted, shunts C53/C54/C58/C59 (70 cm) and C66-C69 (2.4 GHz) DNP, for matching or filtering later.
J7/J9 edge SMAs are hand-fitted (they straddle the board edge); J8/J10 u.FL are placed by JLC. U5/U6 are hand-soldered.
TX and RX modules sit in separate shielded compartments of the lid; RF traces are 50 ohm grounded CPWG with via fences.

USB-A host port (boot stick)

microSD (CM4 Lite only)



Ilim = 6800 / Rset: 6.8k -> 1.0 A (USB), 15k -> 0.45 A (SD).
U8 USBLC6-2SC6: both I/O pin pairs (1/6 = D+, 3/4 = D-) sit on the data lines; layout is flow-through.

SD power switch defaults on (R42 pull-up), as the CM4 datasheet asks when booting from SD.
R43-R47: 47k card pull-ups (CMD, DAT0-3) to the switched SD_VDD. CLK has none.